FORM PTO-1449 (REV. 7-80) | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF DOCUMENTS CITED BY APPLICANT
(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
HIT 2 482-06	09/739,758
APPLICANT: T. WATANABE et al	
FILING DATE: 12/20/00	GROUP: ~~2783~~ 2121

U.S. PATENT DOCUMENTS

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)
	AA	4,994,982	02/1991	Duranton et al			
	AB	4,974,169	11/1990	Engel			
	AC	4,611,299	09/1986	Hori et al			
	AD	4,777,858	01/1989	Wang et al			
	AE	4,847,755	07/1989	Morrison et al			
	AF	4,873,672	10/1989	Etoh et al			
	AG	4,939,696	07/1990	Katsuo et al			
	AH	5,010,477	04/1991	Omada et al			
	AI	5,140,670	08/1992	Chua et al			
	AJ	5,142,665	08/1992	Bigus			
	AK	5,239,654	08/1993	Ing-Simmon et al			

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AL						☐	☐
	AM						☐	☐
	AN						☐	☐
	AO						☐	☐
	AP						☐	☐

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

	AR		Sejnowski et al, "Parallel Networks that Learn to Pronounce English Text", COMPUTER SYSTEMS 1, 1987, pp. 145-168.
	AS		Asou, "Neural Network Processing", Chapters 2 and 3, Sangyo Tosho pub., pp. 39-68, 69-93 and 118-123.
	AT		Advanced Micro Devices, MEMORY PRODUCTS DATA BOOK, Jan. 1989, pp. 4-80, 4-81.

EXAMINER: [signature] DATE CONSIDERED: 2/11/4

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	AA	5,005,121	04/1991	Nakada et al			
	AB	5,163,120	11/1992	Childers et al			
	AC	5,301,340	04/1994	Cook			
	AD	5,023,833	06/1991	Baum			
	AE	5,179,680	01/1993	Colwell			
	AF	5,107,442	04/1992	Weidman			
	AG	5,165,010	11/1992	Masuda			
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	AI	4,471,426	09/1984	McDonough			
	AJ						
	AK						

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	AR	Eberhardt et al, "Design of Parallel Hardware Neural Nework Systems From Customer Analog VLSI 'Building Block' Chips", INTERNATIONAL JOINT CONFERENCE ON NEURAL NETWORKS, June 18-22, 1989, pp. II-183 to II-190.
	AS	Rumelhart et al, "Learning Representations by Back Propagating Errors", NATURE, Vol. 323, October 9, 1986, pp. 533-536.
	AT	Nikkei Microdevices, March 1989, pp. 123-129.

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H	AR		Suzuki et al, "A Study of Regular Architectures for Digital Implementation of Neural Networks", 1989 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, May 8-11, 1989, pp. 82-85.
H	AS		Holler et al, "An Electrically Trainable Artificial Network (ETANN) with 10240 'Floating Gate' Synapses", PROCEEDINGS OF THE INTERNATIONAL ANNUAL CONFERENCE ON NEURAL NETWORKS, 1989, pp. 50-55.
H	AT		Manuel, "Are Artificial Neural Networks Finally Ready for Market?", ELECTRONICS, August 1988, pp. 85-88.

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✓	AR		Sawada et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM", PROCEEDINGS IEEE 1988 CUSTOM INTEGRATED CIRCUIT CONFERENCE, pp. 20.3.1 to 20.3.4.
	AS		
	AT		

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